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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,875	06/22/2001	Natsuki Kushiyama	81790.0204	8040

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,875	KUSHIYAMA, NATSUKI	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-19,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-19,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-22 of U.S. Application 09/887,875 filed on 06/21/2001 are presented for examination. The application claims priority to Japanese Application 2000-188857, filed on 06/23/2000.
2. In the previous Office Action, the Examiner took into account the findings of the Japanese Patent Office in regards to the priority case, Japanese Application 2000-188857. The Applicant submitted the JPO Office Action for Examiner's review on 10/24/1003.
3. In the amendment filed 4/7/2005, the Applicant has rolled up the limitations of dependent claim 5 into independent claim 1, and has rolled up the limitations of dependent claim 20 into independent claim 19. Claims 5 and 20 have been cancelled. Amendments to other claims were in order to remedy informalities that were objected to in the previous Office Action.
4. Applicant's arguments (see pp.10-11 of the Amendment filed on 4/7/05) with respect to the rejections of claim 5 under 35 U.S.C. §103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art. This action is Non-Final.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 2-4 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

   a. The claimed equation in Claim 2, "VREFintn-1 = VREFn-1 + A", is supported in the specification for when A is a negative rational number, but not for when A is a positive rational number.

   b. The claimed equation in Claim 3, "VREFintn-1 = B x VREFn-1", is supported in the specification for when B is a negative rational number, but not for when B is a positive rational number.

   c. The claimed equation in Claim 4, "VREFintn-1 = C X VREFn-1 + D", is supported in the specification for when C is a positive rational number and when D is a negative rational number, but not for when C is negative or D is positive.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The prior art used for these rejections is as follows:

   a. Yoshida, U.S. Patent 5,367,487. (Henceforth referred to as "**Yoshida**").

   b. Patel et al., U.S. Patent 6,025,737. (Henceforth referred to as "**Patel**").

9. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

10. Claims 1-4, 6-19, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Patel.

11. The Yoshida reference teaches the following limitations:

> 1. A semiconductor integrated circuit comprising:
>
> a reference potential conversion circuit which is supplied with n-1 (n is 2 or larger natural number) external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and converts external reference potentials to generate n-1 internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) differing from external reference potentials and having a relationship with regard to the n-1 external reference potentials,
>
> ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$)

Yoshida teaches (see Fig.9, Items 57 and 58, and col.6, line 57 to col.7, line 6) the use of exactly two "Source Voltage Converting Circuits" that convert the source voltages Vcc and Vss to two internal voltages: Vcc1 and Vcc2.

> an input circuit which is supplied with said internal reference potential ($VREF_{int1}$, $VREF_{int2}$, ... $VREF_{int(n-1)}$) as reference potentials, is supplied with n values of data signals expressed by potentials, and compares a data signal and a reference potential to output a determination result.

Yoshida teaches (see Fig.9, Item 59 and Fig.6, and col.5, line 67 to col.6, line 11) the use of a "switch circuit". The MOSFETS in the circuit in Fig.6 compare the values of data signals Φ and $\underline{\Phi}$ such that "... a desired internal source voltage Vint can be obtained from the source voltage Vcc" (see col.7, lines 27-28).

In regards to the following limitations:

> a storage circuit for holding data, and
>
> a control circuit for changing said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) based on data of a plurality of bits stored in said storage circuit.

Yoshida's "comparator" (See Yoshida, Fig.4, Item 27 and col.5, lines 33-42), which corresponds to the claimed "control circuit", is connected to a "reference potential generating circuit" (See Yoshida, Fig.4, Item 26 and col.5, lines 33-42).

In regards to when n>= 3, Examiner finds this to be a mere duplication of parts. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). See MPEP §2144.04 (VI)(B)

However, Yoshida does not expressly teach that the "storage circuit" connected to the "control circuit" <u>stores a plurality of bits</u>. Yoshida is <u>silent</u> as to whether this "reference potential generating circuit" stores a plurality of bits. Yoshida only teaches that the "reference potential generating circuit" generates a constant voltage V_{r1}.

The Patel reference, on the other hand, expressly teaches a "voltage down converter (VDC)" (see Fig.6, Item 610, and col.7, lines 12-61; and Fig.13, Item 1330, and col.20, lines 21-52). Patel expressly teaches the following (see col.7, lines 54-61):

> "There are many techniques for implementing the programmable options feature of the present invention besides mask programmable options. These include, and are not limited to, laser programmable options, fuses, antifuse, in-system programmable (ISP) options, reprogrammable cells such as EEPROM, Flash, EPROM, and SRAM, and many others."

It is inherent that these programmable technologies store sequences of bits.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Yoshida with those of Patel, because both are directed to "voltage down converters."

12. In regards to Claim 2,

> 2. The semiconductor integrated circuit according to claim 1, wherein said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) is expressed by $VREF_{int(n-1)} = VREF_{n-1} + A$ (n is 2 or larger natural number and A is a rational number except 0).

Patel expressly teaches (see col.7, lines 18–28) the following:

> "As shown in Fig.6, the power supply is 5 volts. This voltage is converted using on-chip circuitry to a lower voltage of 3.3 volts. This conversion may be performed using a voltage down converter (VDC) 610. ... Further, in interface 411, the core 3.3-volt signals may be converted to5-volt output signals by circuitry such as level-shifting pre-drivers. The circuits used to perform the conversion in the interface are connected to the 5-volt supply voltage."

13. In regards to Claim 3,

> 3. The semiconductor integrated circuit according to claim 1, wherein said relationship between said

> external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) is expressed by $VREF_{int(n-1)} = B \times VREF_{n-1}$ (n is 2 or larger natural number and B is a rational number except 0).

On the other hand, Reference 3 (see Fig.1) teaches a voltage dividing circuit comprising resistance elements R1, R2, R3 and R4 producing a desired voltage "VREFA" from a "reference potential".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Reference 1 with those of Reference 3, because it was old and well known to employ a voltage dividing circuit that uses resistance elements to produce, based on a reference voltage, a voltage different from the reference voltage..

14. In regards to Claim 4,

> 4. The semiconductor integrated circuit according to claim 1, wherein said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) is expressed by $VREF_{int(n-1)} = C \times VREF_{n-1} + D$ (n is 2 or larger natural number and, C and D are rational numbers except 0).

The Patel reference expressly teaches a "voltage down converter (VDC)" (see Fig.6, Item 610, and col.7, lines 12-61; and Fig.13, Item 1330, and col.20, lines 21-52). Patel expressly teaches the following (see col.7, lines 54-61):

"There are many techniques for implementing the programmable options feature of the present invention besides mask programmable options. These include, and are not limited to, laser programmable options, fuses, antifuse, in-

system programmable (ISP) options, reprogrammable cells such as EEPROM, Flash, EPROM, and SRAM, and many others."

15. In regards to Claim 6,

> 6. The semiconductor integrated circuit according to claim 1, wherein
> said storage circuit for holding data of a plurality of bits is a one-time programmable storage circuit, and
> said relationship between said external reference wherein potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) is changed based on data of a plurality of bits stored in said storage circuit.

The Patel reference expressly teaches a "voltage down converter (VDC)" (see Fig.6, Item 610, and col.7, lines 12-61; and Fig.13, Item 1330, and col.20, lines 21-52). Patel expressly teaches the following (see col.7, lines 54-61):

> "There are many techniques for implementing the programmable options feature of the present invention besides mask programmable options. These include, and are not limited to, laser programmable options, fuses, antifuse, in-system programmable (ISP) options, reprogrammable cells such as EEPROM, Flash, EPROM, and SRAM, and many others."

16. In regards to Claim 7,

> 7. The semiconductor integrated circuit according to claim 6, wherein
> said storage circuit includes a laser beam blown type fuse for specifying data of a plurality of bits to be held depending on whether a laser beam disconnects the fuse, and wherein
> said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) is changed based on data of a plurality of bits stored in said laser beam blown type fuse.

The Patel reference expressly teaches a "voltage down converter (VDC)" (see Fig.6, Item 610, and col.7, lines 12-61; and Fig.13, Item 1330, and col.20, lines 21-52). Patel expressly teaches the following (see col.7, lines 54-61):

"There are many techniques for implementing the programmable options feature of the present invention besides mask programmable options. These include, and are not limited to, laser programmable options, fuses, antifuse, in-system programmable (ISP) options, reprogrammable cells such as EEPROM, Flash, EPROM, and SRAM, and many others."

17. In regards to Claim 8,

> 8. The semiconductor integrated circuit according to claim 6, wherein
> said storage circuit includes an electric current blown type fuse for specifying data of a plurality of bits to be held depending on whether an electric current disconnects the fuse, and
> said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) is changed based on data of a plurality of bits stored in said electric current blown type fuse.

The Patel reference expressly teaches a "voltage down converter (VDC)" (see Fig.6, Item 610, and col.7, lines 12-61; and Fig.13, Item 1330, and col.20, lines 21-52). Patel expressly teaches the following (see col.7, lines 54-61):

"There are many techniques for implementing the programmable options feature of the present invention besides mask programmable options. These include, and are not limited to, laser programmable options, fuses, antifuse, in-system programmable (ISP) options, reprogrammable cells such as EEPROM, Flash, EPROM, and SRAM, and many others."

18. In regards to Claim 9,

> 9. The semiconductor integrated circuit according to claim 6, wherein
> said storage circuit includes a dielectric film breakdown type fuse for specifying data of a plurality of bits to be held depending on whether a voltage breakdowns a dielectric film of the dielectric film breakdown type fuse, and
> said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) is changed based on data of a plurality of bits stored in said dielectric film breakdown type fuse.

The Patel reference expressly teaches a "voltage down converter (VDC)" (see Fig.6, Item 610, and col.7, lines 12-61; and Fig.13, Item 1330, and col.20, lines 21-52). Patel expressly teaches the following (see col.7, lines 54-61):

> "There are many techniques for implementing the programmable options feature of the present invention besides mask programmable options. These include, and are not limited to, laser programmable options, fuses, antifuse, in-system programmable (ISP) options, reprogrammable cells such as EEPROM, Flash, EPROM, and SRAM, and many others."

19. In regards to Claim 10,

> 10. The semiconductor integrated circuit according to claim 5, wherein
> said storage circuit for holding data of a plurality of bits is a re-programmable storage circuit and
> said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$), and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$)is changed based on data of a plurality of bits stored in said storage circuit.

The Patel reference expressly teaches a "voltage down converter (VDC)" (see Fig.6, Item 610, and col.7, lines 12-61; and Fig.13, Item 1330, and col.20, lines 21-52). Patel expressly teaches the following (see col.7, lines 54-61):

> "There are many techniques for implementing the programmable options feature of the present invention besides mask programmable options. These include, and are not limited to, laser programmable options, fuses, antifuse, in-system programmable (ISP) options, reprogrammable cells such as EEPROM, Flash, EPROM, and SRAM, and many others."

20. In regards to Claim 11,

> 11. The semiconductor integrated circuit according to claim 10, wherein
> said storage circuit includes a semiconductor memory circuit for specifying data of a plurality of bits to be held, and
> said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) is changed based on data of a plurality of

bits stored in said semiconductor memory circuit.

The Patel reference expressly teaches a "voltage down converter (VDC)" (see Fig.6, Item 610, and col.7, lines 12-61; and Fig.13, Item 1330, and col.20, lines 21-52). Patel expressly teaches the following (see col.7, lines 54-61):

> "There are many techniques for implementing the programmable options feature of the present invention besides mask programmable options. These include, and are not limited to, laser programmable options, fuses, antifuse, in-system programmable (ISP) options, reprogrammable cells such as EEPROM, Flash, EPROM, and SRAM, and many others."

21. In regards to Claim 12,

> 12. The semiconductor integrated circuit according to claim 10, wherein
> said storage circuit includes a register for specifying data of a plurality of bits to be held, and
> said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) is changed based on data of a plurality of bits stored in said register.

The Patel reference expressly teaches a "voltage down converter (VDC)" (see Fig.6, Item 610, and col.7, lines 12-61; and Fig.13, Item 1330, and col.20, lines 21-52). Patel expressly teaches the following (see col.7, lines 54-61):

> "There are many techniques for implementing the programmable options feature of the present invention besides mask programmable options. These include, and are not limited to, laser programmable options, fuses, antifuse, in-system programmable (ISP) options, reprogrammable cells such as EEPROM, Flash, EPROM, and SRAM, and many others."

22. In regards to Claim 13,

> 13. The semiconductor integrated circuit according to claim 1, wherein said storage circuit comprises a first storage circuit for holding data of a plurality of bits, and a second storage circuit for holding data of a plurality of bits, and wherein
> said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ...

> $VREF_{int(n-1)}$) is changed based on data of a plurality of bits stored in said first storage circuit or said second storage circuit.

In regards to the multiple storage circuits, Examiner finds this to be a mere duplication of parts. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). See MPEP §2144.04 (VI)(B).

23. In regards to Claim 14,

> 14. The semiconductor integrated circuit according to claim 13, further comprising a selection circuit for selecting said first storage circuit or said second storage circuit, and wherein
> said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) is changed based on data of a plurality of bits stored in said first storage circuit or said second storage circuit selected by said selection circuit.

In regards to when multiple storage circuits, Examiner finds this to be a mere duplication of parts. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). See MPEP §2144.04 (VI)(B).

24. Claims 15 are rejected on the same grounds as Claim 14, because they claim the same limitations.

25. In regards to Claim 16,

> 16. The semiconductor integrated circuit according to claim 1, wherein said input circuit compares an input data signal with the reference potential having n-1 values at the timing of a clock signal's leading and trailing edge or either edge and outputs a comparison result.

See Yoshida, Fig.11, and associated text.

26. Claims 17-18 are rejected on the same grounds as Claim 16, because they claim the same limitations.

27. In regards to Claim 19,

> 19. A semiconductor apparatus system, comprising:
>
> a plurality of semiconductor integrated circuits which is mounted on said motherboard and includes a reference potential conversion circuit connected to said external reference signal line, supplied with n-1 (n is 2 or larger natural number) external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$), and generating other potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) differing from said external reference potentials and further includes
>
> an input circuit supplied with output potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) from said reference potential conversion circuit as reference potentials, supplied with a data signal from said data signal line, comparing the input data signal with reference potentials having n-1 values for determination, and generating a determination result.
>
> a storage circuit for holding data, and
>
> a control circuit for changing said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) based on data of a plurality of bits stored in said storage circuit.

The above cited limitations are analogous to the limitations in Claim 1, and are rejected on the same grounds. The following limitations, however, are not in Claim 1:

> a motherboard including an input/output terminal section and a data signal line and an external reference signal line connected to this input/output terminal section, and

Official Notice is given that it was old and well known at the time the invention was made to place circuits on motherboards, and laying the input/output terminal section and signal lines on the motherboard.

It would have been obvious to one of ordinary skill in the art to modify the teachings of Yoshida in view of Patel, because it was old and well know at the time the invention was made to place integrated circuits on motherboards..

28. In regards to Claim 21,

> 21. The semiconductor integrated circuit according to claim 19, wherein
> said storage circuit further comprises a first storage circuit for holding data of a plurality of bits, and a second storage circuit for holding data of a plurality of bits, and wherein
> said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) is changed based on data of a plurality of bits stored in said first storage circuit or said second storage circuit.

In regards to the multiple storage circuits, Examiner finds this to be a mere duplication of parts. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). See MPEP §2144.04 (VI)(B).

29. In regards to Claim 22,

> 22. The semiconductor integrated circuit according to claim 19, wherein
> said semiconductor integrated circuit further comprises a selection circuit for selecting said first storage circuit or said second storage circuit, and wherein
> said relationship between said external reference potentials ($VREF_1$, $VREF_2$, ..., $VREF_{n-1}$) and said internal reference potentials ($VREF_{int(1)}$, $VREF_{int(2)}$, ... $VREF_{int(n-1)}$) is changed based on data of a plurality of bits stored in said first storage circuit or said second storage circuit selected by said selection circuit.

In regards to the multiple storage circuits, Examiner finds this to be a mere duplication of parts. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). See MPEP §2144.04 (VI)(B).

Response to Amendment

Re: Claim Objections

30. Applicant's amendment to the claims has overcome the claim objection. The claim objection has therefore been withdrawn.

Re: Claim Rejections - 35 USC § 102 and §103

31. Examiner has found Applicant's arguments to be persuasive. New art rejections have been applied.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (703) 872-9306, or mailed to:

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P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
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Randolph Building
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Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

June 24, 2005

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100